U	L	Document ID	Issue Date	Pages	Title	Current OR	Current XRef	Retrieval C	Inventor	S	O	P				Ima
1		US 20020013918 A1	20020131	68	Devices, systems and methods for mode driven stops	714/30		712/227	Swoboda, Gary L. et al.	☑						US
2		US 20030063517 A1	20030403	9	Integrated circuits with parallel self-testing	365/230.05			Jain, Raj Kumar	☑						US
3		US 5329471 A	19940712	83	Emulation devices, systems and methods utilizing state	703/23		703/13; 714/28;	Swoboda, Gary L. et al.	☑						US
4		US 5535331 A	19960709	107	Processor condition sensing circuits, systems and	714/45		714/28; 714/30	Swoboda, Gary L. et al.	☑						US
5		US 5621651 A	19970415	109	Emulation devices, systems and methods with distributed	703/23		703/13	Swoboda, Gary L.	☑						US
6		US 5752069 A	19980512	151	Superscalar microprocessor employing away prediction	712/23		711/128; 711/204;	Roberts, James S. et al.	☑						US
7		US 5781789 A	19980714	146	Superscalar microprocessor employing a parallel mask	712/23		712/205; 712/210;	Narayan, Rammohan	☑						US
8		US 5805792 A	19980908	108	Emulation devices, systems, and methods	714/28		714/25	Swoboda, Gary L. et al.	☑						US
9		US 5822559 A	19981013	150	Apparatus and method for aligning variable	712/214		712/213	Narayan, Rammohan et al.	☑						US
10		US 5826071 A	19981020	146	Parallel mask decoder and method for generating said	712/224		712/23	Narayan, Rammohan	☑						US
11		US 5841670 A	19981124	87	Emulation devices, systems and methods with distributed	703/23		714/731	Swoboda, Gary L.	☑						US
12		US 5854921 A	19981229	145	Stride-based data address prediction structure	712/239		712/1; 712/23	Tickett, James K.	☑						US
13		US 5859991 A	19990112	155	Parallel and scalable method for identifying valid	712/204			Narayan, Rammohan	☑						US
14		US 5860104 A	19990112	149	Data cache which speculatively updates a	711/137		711/126; 711/204;	Witt, David B. et al.	☑						US
15		US 5864707 A	19990126	149	Superscalar microprocessor configured to predict return	712/23		712/228; 712/243	Tran, Thang M. et al.	☑						US
16		US 5875315 A	19990223	100	Parallel and scalable instruction scanning unit	712/204			Narayan, Rammohan	☑						US
17		US 5875324 A	19990223	147	Superscalar microprocessor which delays update of	712/238		712/240	Tran, Thang M. et al.	☑						US
18		US 5870255 A	19990302	137	Update unit for providing a delayed update to a branch	712/240			Tran, Thang M. et al.	☑						US
19		US 5881278 A	19990309	154	Return address prediction system which adjusts the	712/242		712/238	Tran, Thang M. et al.	☑						US
20		US 5892936 A	19990406	140	Speculative register file for storing speculative	712/216		712/212; 712/213;	Tran, Thang M. et al.	☑						US
21		US 5933618 A	19990803	154	Speculative register storage	712/217		712/212;	Tran, Thang M. et al.							US

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13		US 5859991 A	19990112	155	Parallel and scalable method for identifying valid	712/204			Narayan, Rammohan							US
14		US 5860104 A	19990112	149	Data cache which speculatively updates a	711/137	711/126; 711/204;		Witt, David B. et al.							US
15		US 5864707 A	19990126	149	Superscalar microprocessor configured to predict return	712/23	712/228; 712/243		Tran, Thang M. et al.							US
16		US 5875315 A	19990223	180	Parallel and scalable instruction scanning unit	712/204			Narayan, Rammohan							US
17		US 5875324 A	19990223	147	Superscalar microprocessor which delays update of	712/238	712/240		Tran, Thang M. et al.							US
18		US 5878255 A	19990302	137	Update unit for providing a delayed update to a branch	712/240			Tran, Thang M. et al.							US
19		US 5881278 A	19990309	154	Return address prediction system which adjusts the	712/242	712/238		Tran, Thang M. et al.							US
20		US 5892936 A	19990406	140	Speculative register file for storing speculative	712/216	712/212; 712/213;		Tran, Thang M. et al.							US
21		US 5933618 A	19990803	154	Speculative register storage for storing speculative	712/217	712/212; 712/213;		Tran, Thang M. et al.							US
22		US 5935239 A	19990810	144	Parallel mask decoder and method for generating said	712/224	712/213; 712/23;		Narayan, Rammohan							US
23		US 5978907 A	19991102	145	Delayed update register for an array	712/239			Tran, Thang M. et al.							US
24		US 5987561 A	19991116	146	Superscalar microprocessor employing a data cache	711/3	711/128; 711/204;		Witt, David B. et al.							US
25		US 6008821 A	19991228	18	Embedded frame buffer system and synchronization method	345/504	345/519; 345/545		Bright, Arthur Aaron et al.							US
26		US 6014734 A	20000111	150	Superscalar microprocessor configured to predict return	712/23	712/229; 712/229;		Tran, Thang M. et al.							US
27		US 6032268 A	20000229	77	Processor condition sensing circuits, systems and	714/30	714/34; 714/726		Swoboda, Gary L. et al.							US
28		US 6079006 A	20000620	152	Stride-based data address prediction structure	711/213	711/221; 712/237;		Pickett, James K.							US
29		US 6085336 A	20000704	91	Data processing devices, systems and methods with	714/30	714/727		Swoboda, Gary L. et al.							US
30		US 6128025 A	20001003	18	Embedded frame buffer system and synchronization method	345/504	345/519; 345/534;		Bright, Arthur Aaron et al.							US
31		US 6189068 B1	20010213	142	Superscalar microprocessor employing a data cache	711/3	711/118; 711/204;		Witt, David B. et al.							US
32		US 6269436 B1	20010731	153	Superscalar microprocessor configured to predict return	712/23	712/220; 712/229;		Tran, Thang M. et al.							US
33		US 6349392 B1	20020219	64	Devices, systems and methods	714/30	713/601;		Swoboda, Gary L. et al.							US

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